IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re	U.S. Patent Application of)
)
HAN	ZAWA et al.)
	u St. I. (I. milman))
Appli	cation Number: to be assigned)
)
Filed:	Concurrently Herewith)
)
For:	SEMICONDUCTOR MEMORY DEVICE)
	EQUIPPED WITH DUMMY CELLS)
)
Attor	ney Docket No. NITT.0155)

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

The above-referenced application is a continuation of U.S. Serial No. 10/315,938 filed on December 11, 2002, which is a continuation of U.S. Serial No. 09/942,558 filed on August 31, 2001 (which issued on January 28, 2003, as U.S. Patent No. 6,512,714 B). It includes the same disclosure as U.S. patent application Serial No. 10/315,938.

It is understood that the listed references will be considered in the examination of the application and that no separate copies of the same prior art are required to be provided since they were previously cited or transmitted in the foregoing prior application. 37 CFR Section 1.98(d). Form(s) PTO 1449 is enclosed listing references cited by the Examining Attorney and submitted by applicant in the prior applications.

This Information Disclosure Statement is submitted with the above-captioned U.S. continuation application. Accordingly, no fee is due or payable at this time.

The Examiner is requested to acknowledge consideration of the information provided in this paper in accordance with prescribed procedures.

Please charge any additional fees or credit any overpayments in connection with this paper to Deposit Account No. 08-1480.

Respectfully submitted,

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REED SMITH LLP

3110 Fairview Park Drive **Suite 1400** Falls Church, Virginia 22042 (703) 641-4200 September 12, 2003

Form PTO 1449	ATTY. DOCKET NUMBER NITT.0155	SERIAL NUMBER To Be Assigned
U.S. Department of Commerce Patent and Trademark Office	APPLICANT Hanzawa et al	
Information Disclosure Statement by Applicant	FILING DATE Concurrently Herewith	GROUP

U.S. Patent Documents

Examiner	Cited in parent	DOCUMENT	Date	Name	CLASS	SUBC	FILING DATE
Initial		Number				LASS	
	X	4,408,304	10/4/83	Nishizawa et al			5/4/81
	X	6,314,017 B1	11/6/2001	Emori et al			7/21/2000
	X	6,512,714 B2	1/28/2003	Hanzawa et al.			8/31/2001
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Foreign Patent Documents

Examiner	Cited in	DOCUMENT NUMBER	FILING DATE	Country	CLASS	SUB-	TRANSL	ATION
Initial	parent					CLASS	YES	No
	Х	9-213812	1/31/1996	Japan			Abstract	X

Other Documents (Including Author, Title, Date Pertinent Pages, Etc.)

	Cited in parent	Regitz, W. M., "A Three-Transistorcell, 1024-Bit, 500 NS MOS RAM," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 1970, pp. 42-43		
	Cited in parent	Nakazato, Kazuo et al., "Phase-state Low Electron-number Drive Random Access Memory (PLEDM)," IEEE International Solid-State Circuits Conferences, Digest of Technical Papers, 2000, pp. 132-133		
Examiner			DATE CONSIDERED	

EXAMINER: Initial if citation is considered, whether or not citation is in conformance with MPEP 609; draw a line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant